CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

forming a floating gate above the first dielectric layer, the floating gate comprised of a first layer doped with a first type of dopant material and a second layer doped with a second type of dopant material that is opposite the first type of dopant material in the first layer;

forming a second dielectric layer above the floating gate;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

2. The method of claim 1, wherein forming the first layer of said floating gate comprises forming a first polysilicon layer above the dielectric layer.

3. The method of claim 2, wherein forming the first polysilicon layer comprises depositing the first polysilicon layer and introducing dopant atoms of the first type of dopant material into the first polysilicon layer during the deposition process.

4. The method of claim 2, wherein forming the first polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the first type of dopant material into the first polysilicon layer.

5. The method of claim 2, wherein forming the floating gate comprises forming a second polysilicon layer above the first polysilicon layer.

6. The method of claim 5, wherein forming the second polysilicon layer comprises depositing the second polysilicon layer and introducing dopant atoms of the second type of dopant material into the second polysilicon layer during the deposition process.

7. The method of claim 5, wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer.

8. The method of claim 5, wherein forming the floating gate further comprises forming a barrier layer between the first polysilicon layer and the second polysilicon layer.

9. The method of claim 5, wherein forming the first polysilicon layer above the dielectric layer and forming the second polysilicon layer above the first polysilicon layer comprises depositing the first polysilicon layer above the dielectric layer and depositing the second polysilicon layer above the first polysilicon layer.

10. The method of claim 9, wherein forming the first polysilicon layer above the dielectric layer and the second polysilicon layer above the first polysilicon layer further comprises performing a first ion implantation process at a first energy to introduce dopant atoms of the first type of dopant material into the first polysilicon layer and performing a second ion implantation process at a second energy to introduce dopant atoms of the second

type of dopant material into the second polysilicon layer with a second dopant, wherein the first energy is larger than the second energy.

11. The method of claim 10, wherein performing the ion implantation process at the first energy comprises performing the ion implantation process at the first energy such that the ion implant range is at about a mid-point of the first polysilicon layer and a first dopant dose of approximately 10^{10} - 10^{15} atoms/cm^2.

12. The method of claim 11, wherein performing the ion implantation process at the second energy comprises performing the ion implantation process at the second energy such that the ion implant range is at about a mid-point of the second polysilicon layer and a second dopant dose of approximately 10^{13} -10^{16} atoms/cm^2.

13. The method of claim 8, wherein forming the floating gate further comprises forming a barrier layer between the first polysilicon layer and the second polysilicon layer.

14. The method of claim 13, wherein forming the barrier layer comprises forming the barrier layer having a thickness ranging from approximately 10-50 Å.

15. A method of forming a double-doped floating gate, comprising:

forming a first dielectric layer on a semiconductor substrate;

forming a first polysilicon layer above the first dielectric layer;

forming a barrier layer above the first polysilicon layer;

forming a second polysilicon layer above the barrier layer;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

16. The method of claim 15, wherein forming the first polysilicon layer comprises depositing the first polysilicon layer and introducing dopant atoms of the first type of dopant material into the first polysilicon layer during the deposition process.

17. The method of claim 15, wherein forming the first polysilicon layer comprises introducing dopant atoms of the first type of dopant material into the first polysilicon layer to a first dopant concentration of approximately 10^{15} - 10^{20} atoms/cm^3.

18. The method of claim 15, wherein forming the first polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the first type of dopant material into the first polysilicon layer.

19. The method of claim 18, wherein forming the first polysilicon layer comprises introducing dopant atoms of the first type of dopant material into the first polysilicon layer to a first dopant concentration of approximately 10^{15} - 10^{20} atoms/cm^3.

20. The method of claim 15, wherein forming the second polysilicon layer comprises depositing the second polysilicon layer and introducing dopant atoms of the second type of dopant material into the second polysilicon layer during the deposition process.

21. The method of claim 20, wherein forming the second polysilicon layer comprises introducing dopant atoms of the second type of dopant material into the second polysilicon layer to a second dopant concentration of approximately 10^{18} - 10^{21} atoms/cm^3.

22. The method of claim 15, wherein forming the second polysilicon layer comprises performing an ion implantation process to introduce dopant atoms of the second type of dopant material into the second polysilicon layer.

23. The method of claim 22, wherein forming the second polysilicon layer comprises introducing dopant atoms of the second type of dopant material into the second polysilicon layer to a second dopant concentration of approximately 10^{18} - 10^{21} atoms/cm^3.

24. A method, comprising:

forming a first dielectric layer on a semiconductor substrate;

depositing a first polysilicon layer above the first dielectric layer;

forming a barrier layer above the first polysilicon layer;

depositing a second polysilicon layer above the barrier layer;

performing a first ion implantation process to introduce a first type of dopant material into the first polysilicon layer using a first dopant dose of approximately 10^{10} - 10^{15} ions/cm^2 at a first energy;

performing a second ion implantation process to introduce a second type of dopant material into the second polysilicon layer using a second dopant dose of approximately 10^{13} - 10^{16} ions/cm^2 at a second energy, wherein the first energy is larger than the second energy;

forming a second dielectric layer above the second polysilicon layer;

forming a control gate above the second dielectric layer; and

forming a source and a drain in the substrate.

25. The method of claim 24, wherein performing the first ion implantation process comprises performing the first ion implantation process at the first energy such that an ion implant range is at about a mid-point of the first polysilicon layer.

26. The method of claim 24, wherein performing the first ion implantation process comprises performing the first ion implantation process to introduce the first type of dopant material to a first dopant concentration of approximately 10^{15} - 10^{20} atoms/cm^3.

27. The method of claim 24, wherein performing the second ion implantation process comprises performing the second ion implantation process at the second energy such that an ion implant range is at about a mid-point of the second polysilicon layer.

28. The method of claim 24, wherein performing the second ion implantation process comprises performing the second ion implantation process to introduce the second type of dopant material to a second dopant concentration of approximately 10^{18} - 10^{21} atoms/cm^3.

29. An apparatus, comprising:

a first dielectric layer formed on a semiconductor substrate;

a double-doped floating gate formed above the dielectric layer;

a second dielectric layer formed above the double-doped floating gate;

a control gate formed above the second dielectric layer; and

a source and a drain formed in the substrate.

30. The apparatus of claim 29, wherein the double-doped floating gate comprises a first doped polysilicon layer formed above the first dielectric layer and a second doped polysilicon layer above the first polysilicon layer.

31. The apparatus of claim 30, wherein the first doped polysilicon layer is doped to a first dopant concentration of about 10^{15} to 10^{20} atoms/cm^3.

32. The apparatus of claim 31, wherein the second doped polysilicon layer is doped to a second dopant concentration of about 10^{18} to 10^{21} atoms/cm^3 with a dopant material having a dopant type opposite to that of the first dopant.

33. The apparatus of claim 30, wherein the second doped polysilicon layer is doped to a second dopant concentration of about 10^{18} to 10^{21} atoms/cm^3.

34. The apparatus of claim 29, wherein the double-doped floating gate comprises a barrier layer formed above the first polysilicon layer and below the second polysilicon layer.